AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) An image processor comprising:

a plurality of processors processing respective portions of the same input image data in parallel with each other and outputting respective processed portions of said input image data; [[and]]

an address memory accepting and storing address information related to a position of each portion of said input image data within said input image data for each respective portion of image data which has been processed by said plurality of processors[[.]];

input means inputting image data subjected to processing in synchronization with a first external device, and

output means outputting said image data processed in said plurality of processors and said address information stored in said address memory in synchronization with a second external device.

2. (Original) The image processor in accordance with claim 1, further comprising:

an image memory storing said image data output from said plurality of processors, and

read means reading said image data from said image memory on the basis of said address information stored in said address memory.

3. (Original) The image processor in accordance with claim 1, further comprising an image memory storing said image data output from said plurality of processors along the sequence of addresses on the basis of said address information stored in said address memory.

4. (Canceled)

5. (Previously Presented) The image processor in accordance with claim 1, wherein said plurality of processors also output arrangement information corresponding to said processed portions of said image data.

6. (Previously Presented) An image processor comprising:

a plurality of processors performing prescribed processing on a plurality of data divided from single image data respectively;

a first memory accepting and storing arrangement information in said single image data for said plurality of divided data, said arrangement information for each of said plurality of divided data being associated with whichever processor performs the prescribed processing of the divided data; and

a controller restoring a single image from said plurality of data processed in said plurality of processors in accordance with said arrangement information.

7. (Original) The image processor in accordance with claim 6, further including a second memory storing said data processed in said plurality of processors, wherein said controller reads said data from said second memory in sequence along said arrangement information and restores said image.

8. (Previously Presented) The image processor in accordance with claim 6, further including an image memory, wherein said controller stores processed data in positions of said image memory corresponding to said arrangement information.

9. (Original) The image processor in accordance with claim 6, wherein said first memory is provided in correspondence to each of said plurality of processors.

10. (Currently Amended) The image processor in accordance with claim [[9]] 6, wherein said plurality of processors also output arrangement information corresponding to processed said data when outputting said data.

11. (Previously Presented) An image processing method including steps of:

dividing input image data into a plurality of image data;

storing information indicating arrangement of said divided image data relative to said input image;

performing image processing on said divided image data with a plurality of processors;

outputting said processed data as well as said information indicating arrangement of said divided data; and

restoring a single image from said processed data in accordance with said information indicating arrangement of said divided data,

wherein each of said plurality of processors processes plural portions of said divided image data, and information indicating arrangement of each divided portion of said image data is associated with whichever processor processes the corresponding divided portion.

12. (Previously Presented) An image processor comprising:

first and second processors having:

an input image data port and an input image address port, for inputting, respectively, image data corresponding to a portion of an image and a position of the image data within the image; and

an output image data port and an output image address port for outputting, respectively, processed image data corresponding to a portion of a processed image and a position of said processed image data within the processed image; and

a data flow control, coupled to said first and second processors, for coordinating the operation thereof so that each of said first and second processors process plural portions of said input image and said first and second processors processes said plural portions asynchronously with respect to each other.

13. (Previously Presented) The image processor of claim 12, further comprising:

an output image data memory; and

an output image address memory, the output image address memory for storing a position of the image data in the output image data memory relative to the image.

14. (Currently Amended) An image processor ~~The image processor in accordance with claim 1, further~~ comprising:

a plurality of processors processing respective portions of the same input image data in parallel with each other and outputting respective processed portions of said input image data; and

an address memory accepting and storing address information related to a position of each portion of said input image data within said input image data for each respective portion of image data which has been processed by said plurality of processors;

an image memory storing said image data output from said plurality of processors, and

a reader reading said image data from said image memory on the basis of said address information stored in said address memory.

15. (Currently Amended) An image processor ~~The image processor in accordance with claim 1, further~~ comprising:

a plurality of processors processing respective portions of the same input image data in parallel with each other and outputting respective processed portions of said input image data; and

an address memory accepting and storing address information related to a position of each portion of said input image data within said input image data for each respective portion of image data which has been processed by said plurality of processors;

an input unit inputting image data subjected to processing in synchronization with a first external device, and

an output unit outputting said image data processed in said plurality of processors and said address information stored in said address memory in synchronization with a second external device.

16. (Currently Amended) An image processor comprising: ~~The image processor in accordance with claim 1,~~

a plurality of processors processing respective portions of the same input image data in parallel with each other and outputting respective processed portions of said input image data; and

an address memory accepting and storing address information related to a position of each portion of said input image data within said input image data for each respective portion of image data which has been processed by said plurality of processors;

wherein said address information is stored so that said address information is associated with whichever processor of the plurality of processors processed the portion of said input image data related to the address information.